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GB 1533644
GB 1501018
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(54) **Shielding semiconductor integrated circuit devices from light**

(57) A semiconductor integrated circuit device, e.g. for an electronic watch, includes an oscillator circuit unit having MISFET type circuit elements Q_1, Q_2, Q_3, Q_4, a capacitor C_3 and a protection resistor RD which is covered with an aluminum light-shielding film 9. As a result, stable operation of the oscillator circuit can be ensured irrespective of any external light, e.g. during adjustment of the oscillation frequency before the integrated circuit is placed in the watch case. The individual circuit elements may have separate shielding films, instead of the overall film 9, and in some embodiments these are formed by enlarging aluminum interconnection films 13, 14, 20, 28, 29, 30, 31.

FIG. 5

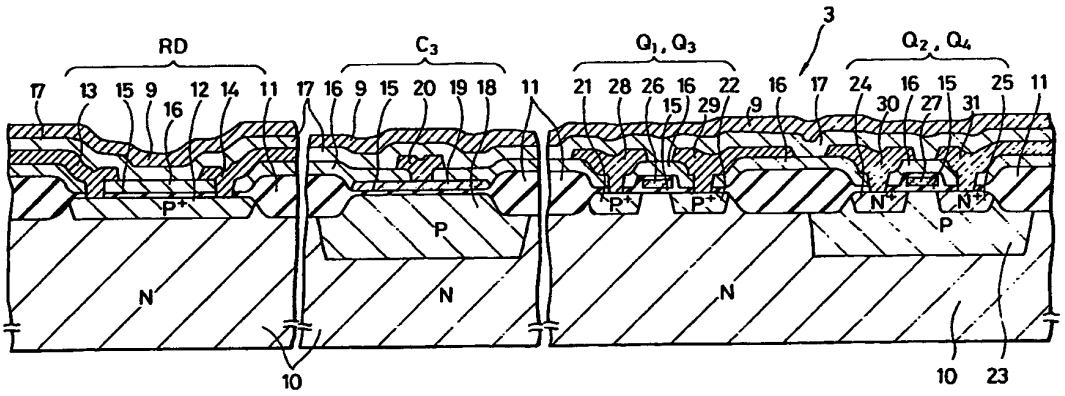

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FIG. 1

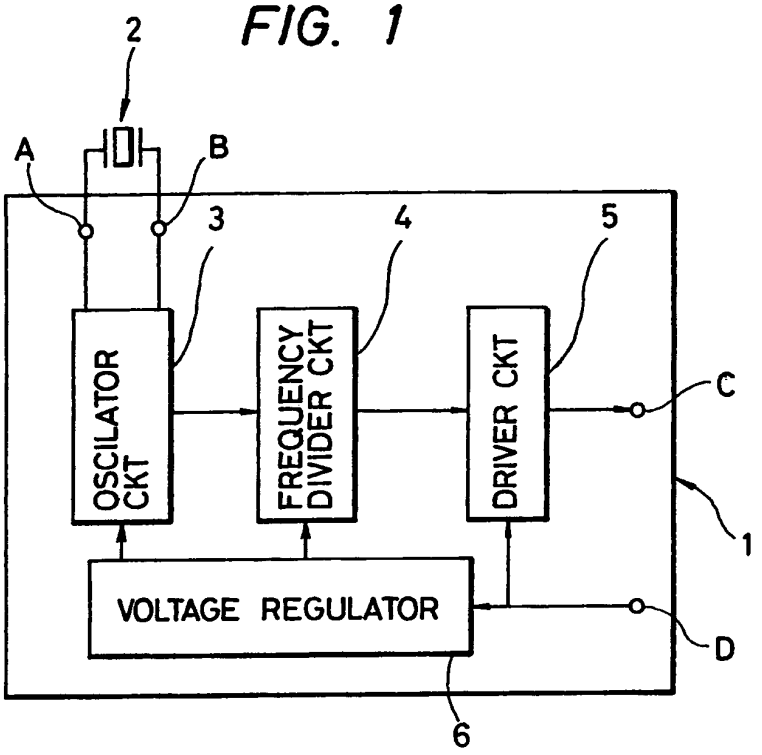

2
A
B
3
4
5
OSCILATOR CKT
FREQUENCY DIVIDER CKT
DRIVER CKT
C
1
VOLTAGE REGULATOR
D
6

FIG. 2

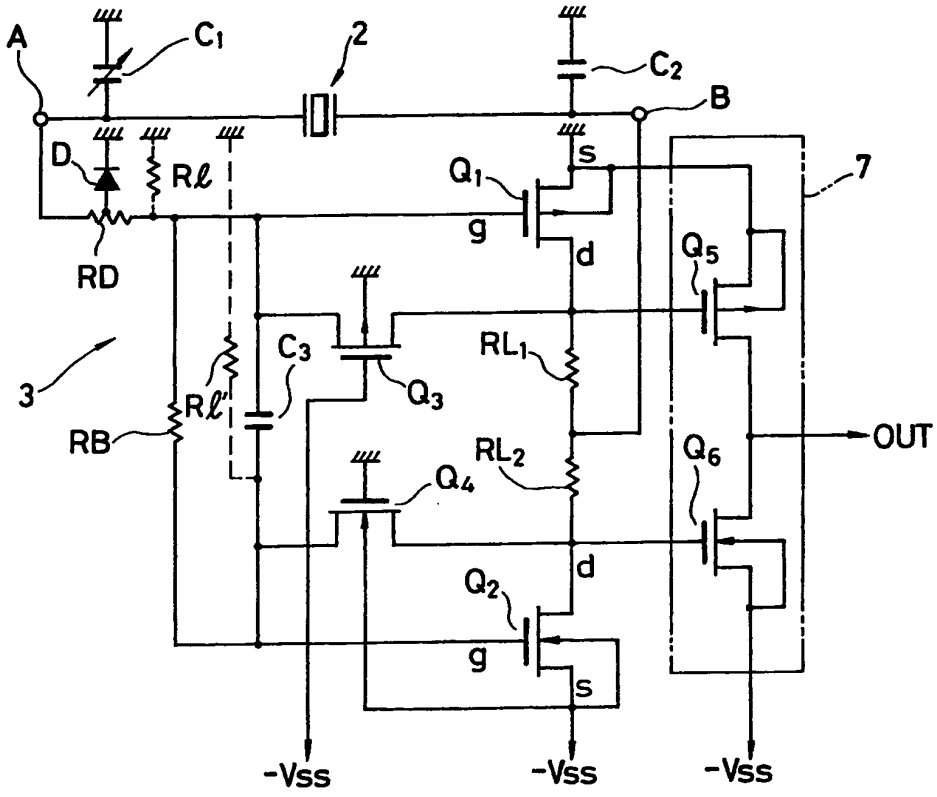

A
C1
2
C2
B
D
Rℓ
RD
Q1
s
g
d
7
Q5
3
C3
Q3
RL1
Rℓ'
RB
OUT
Q6
RL2
Q4
d
Q2
g
s
-Vss
-Vss
-Vss

FIG. 3

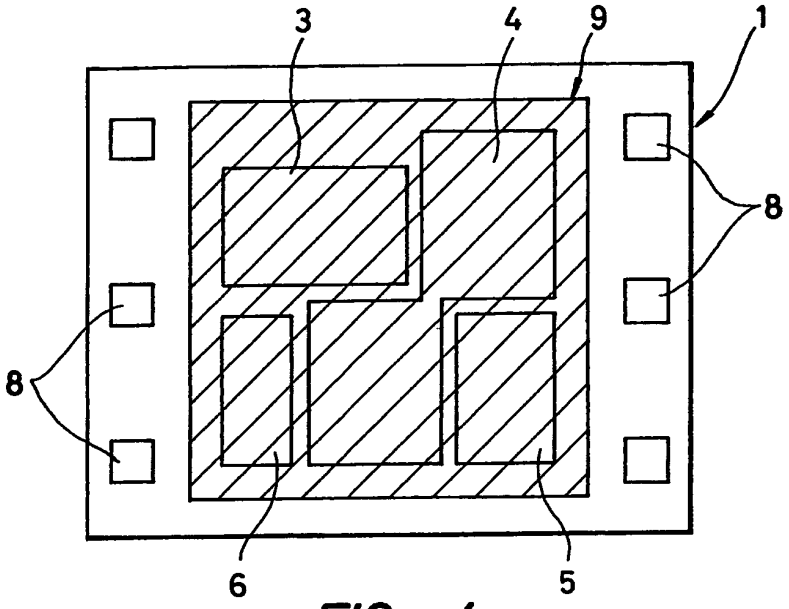


FIG. 4

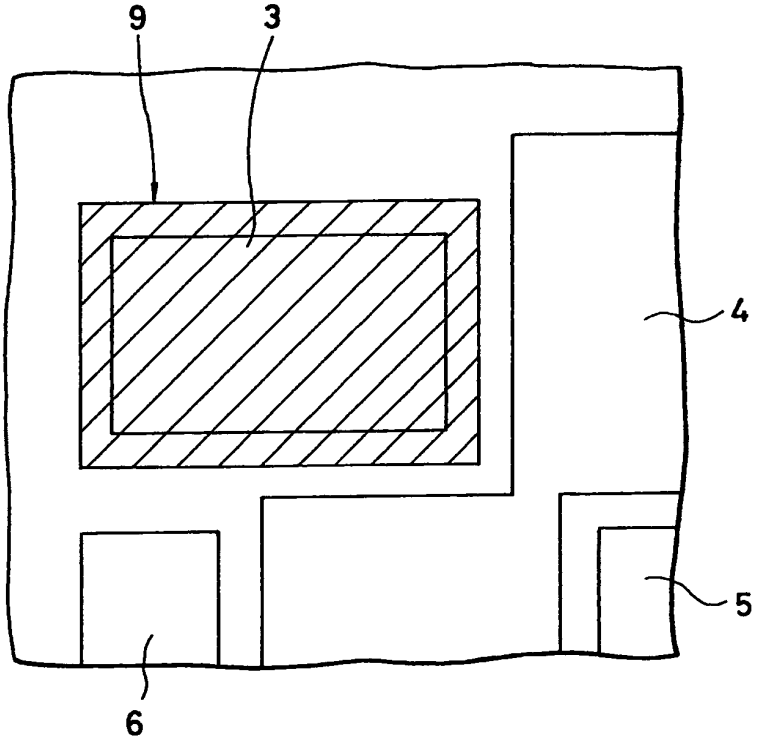


FIG. 5

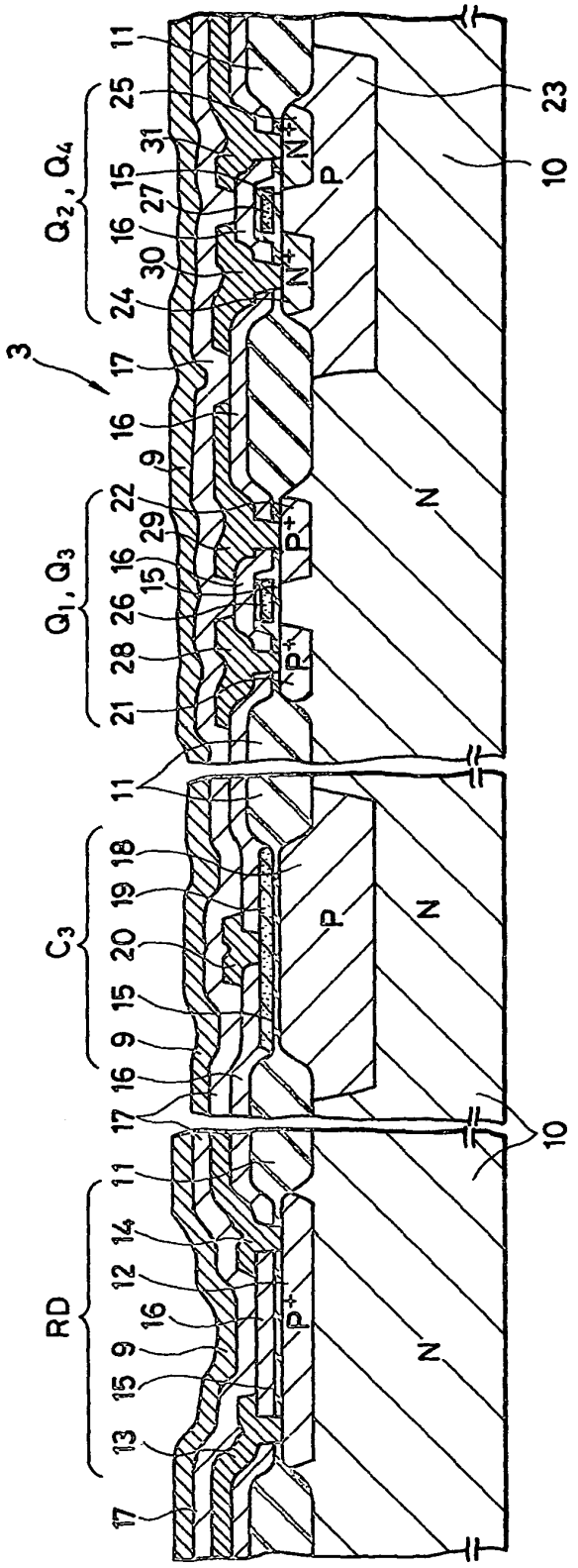

3
Q2, Q4
Q1, Q3
C3
RD
N+
P+
P
N
11
25
31
15
27
16
30
24
17
22
29
26
28
21
18
19
20
9
12
14
13
23
10

FIG. 6

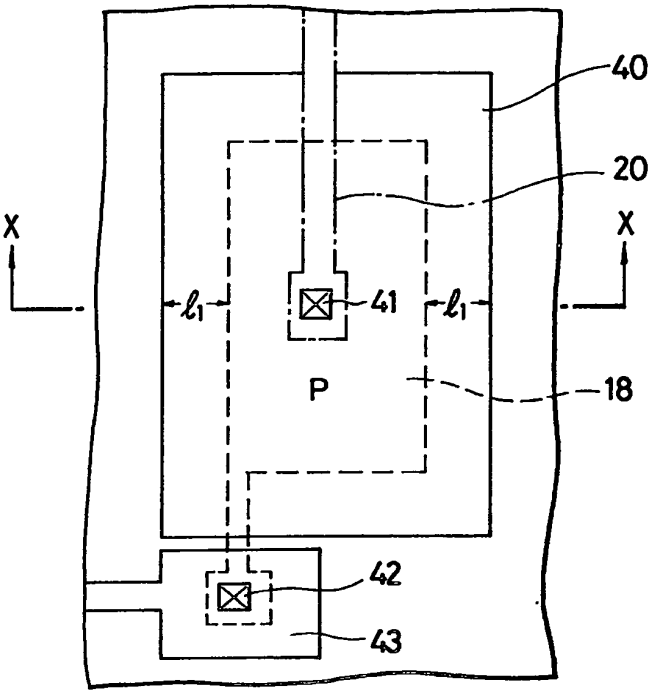

40
20
X
X
ℓ_1
41
ℓ_1
P
18
42
43

FIG. 7

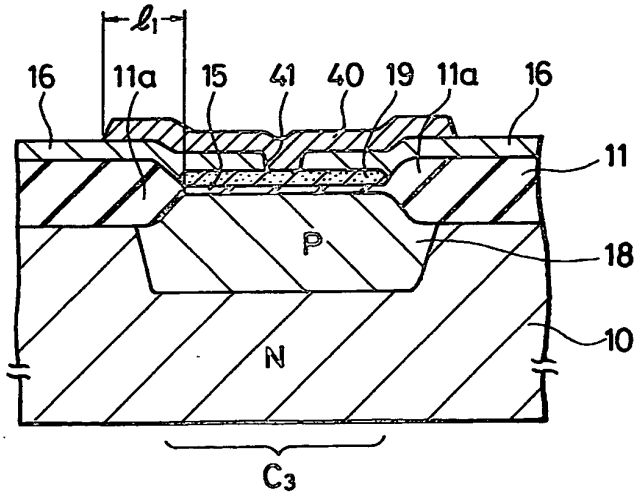

ℓ_1
16
11a
15
41
40
19
11a
16
11
P
18
N
10
C_3

FIG. 8

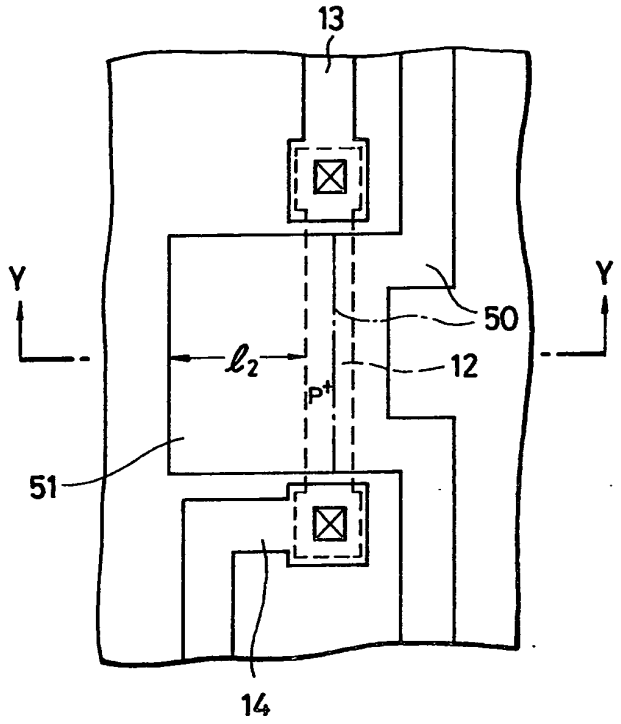


FIG. 9

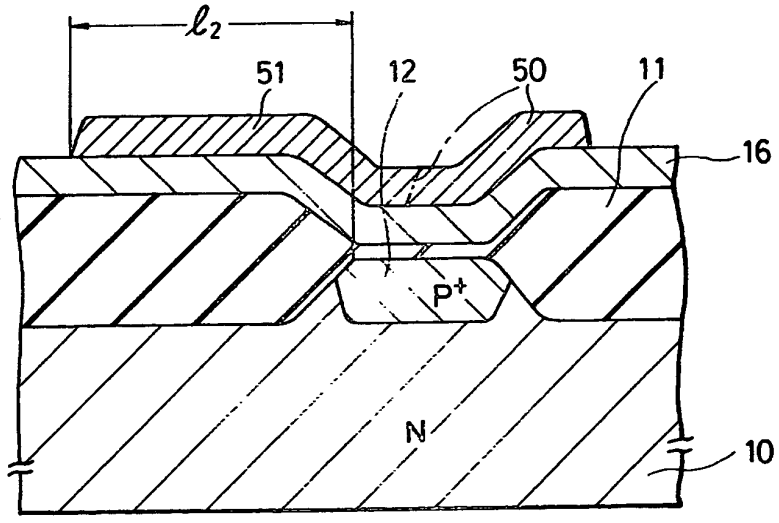


FIG. 10

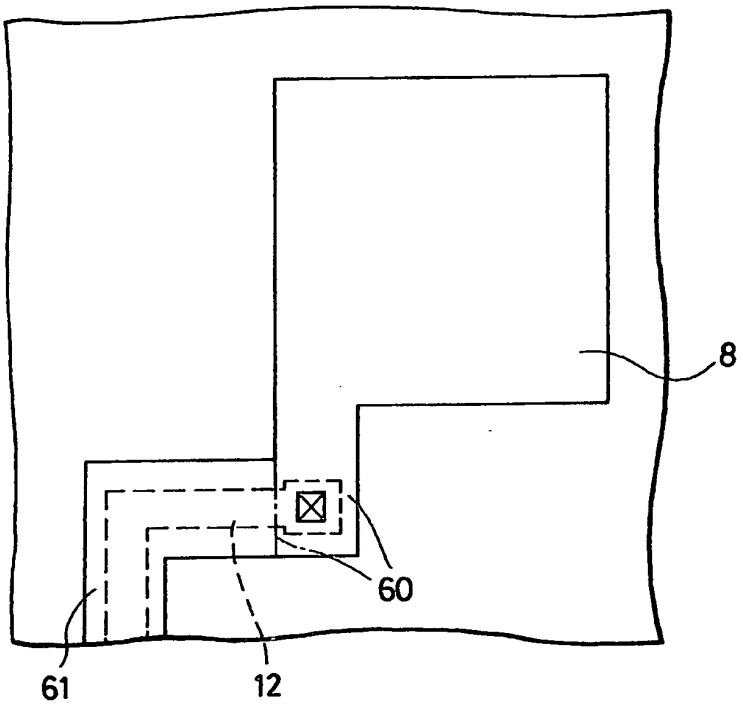


FIG. 11

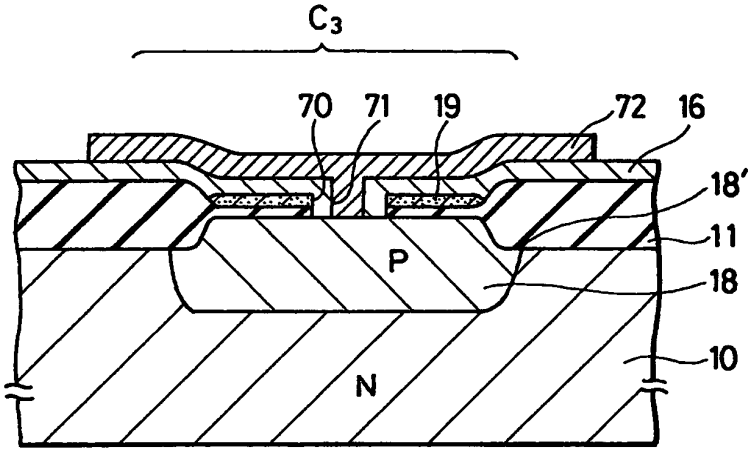


FIG. 12

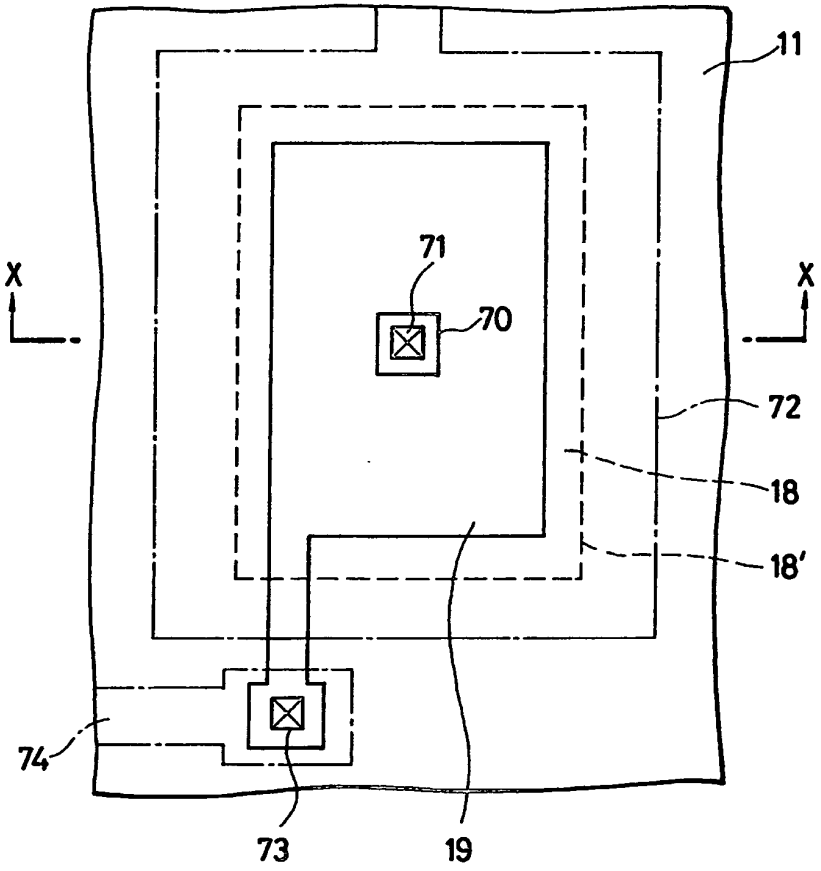


FIG. 13

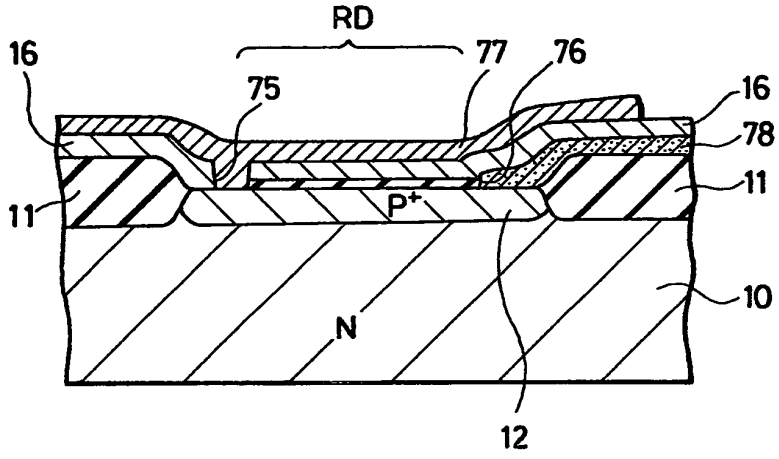


FIG. 14

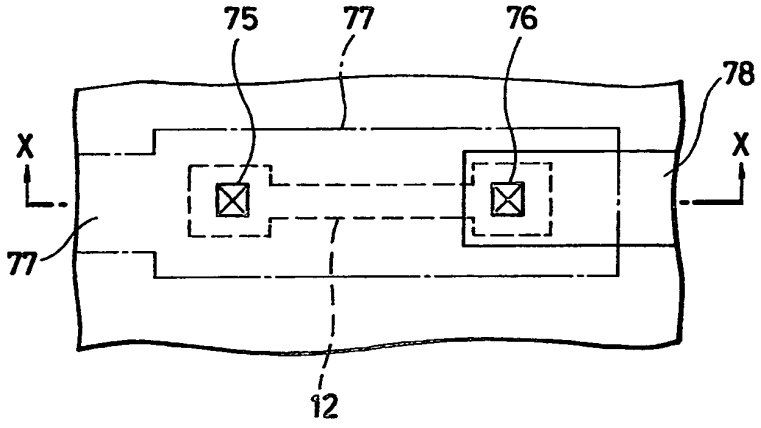


FIG. 15

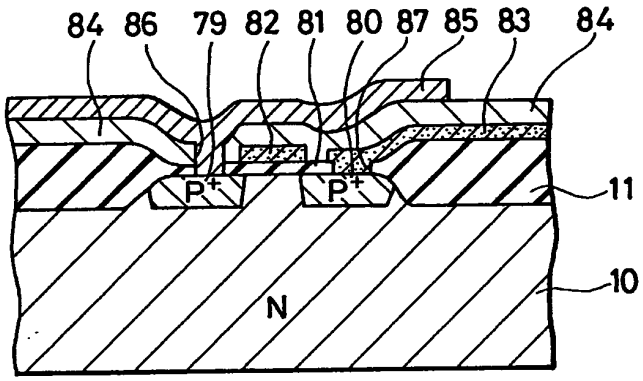


FIG. 16

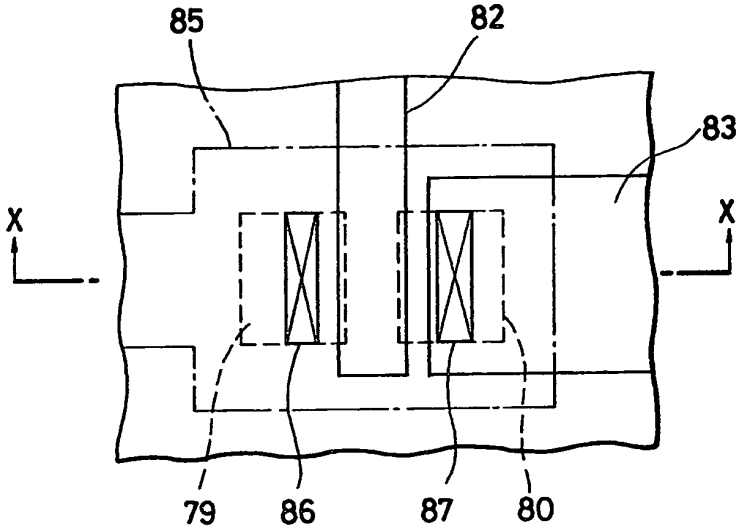


FIG. 17

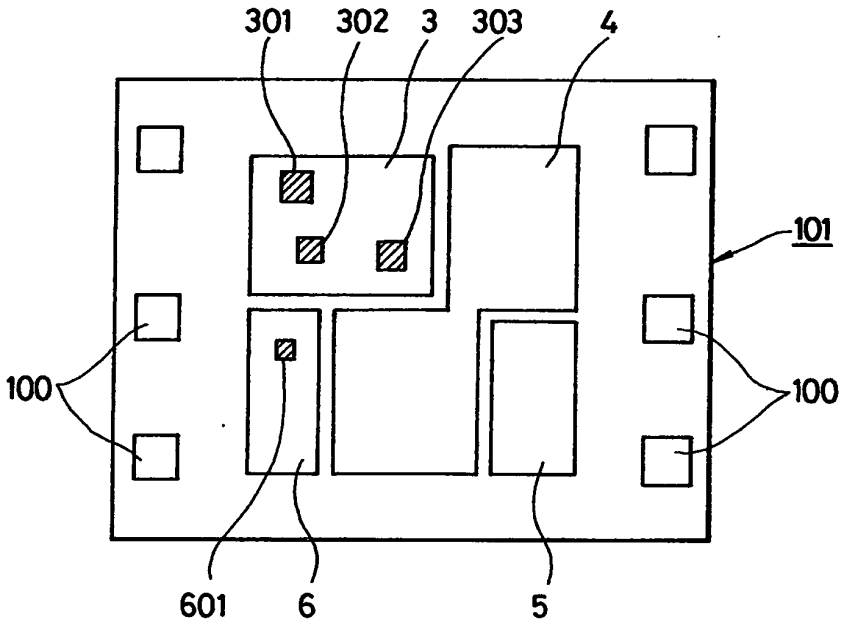


FIG. 18

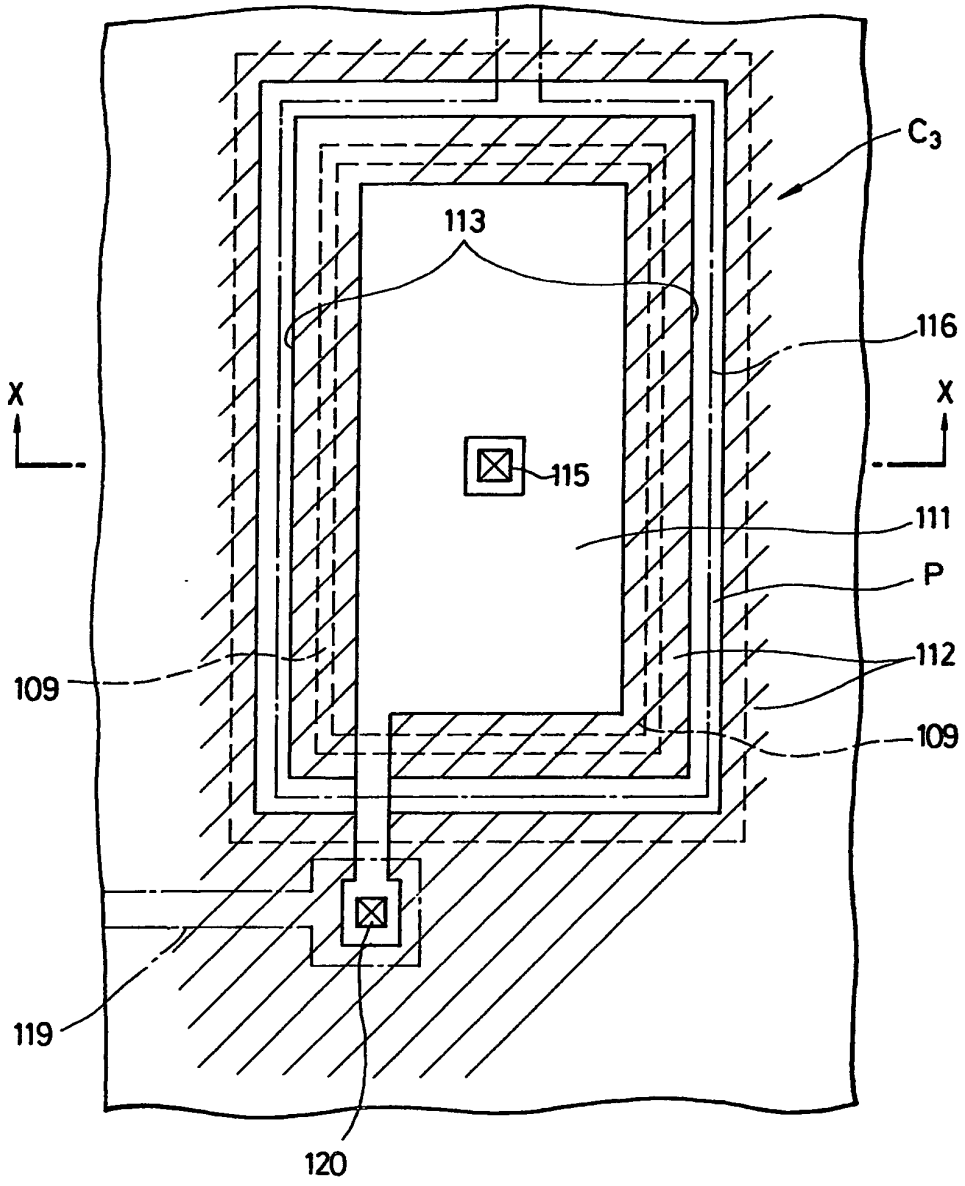


FIG. 19

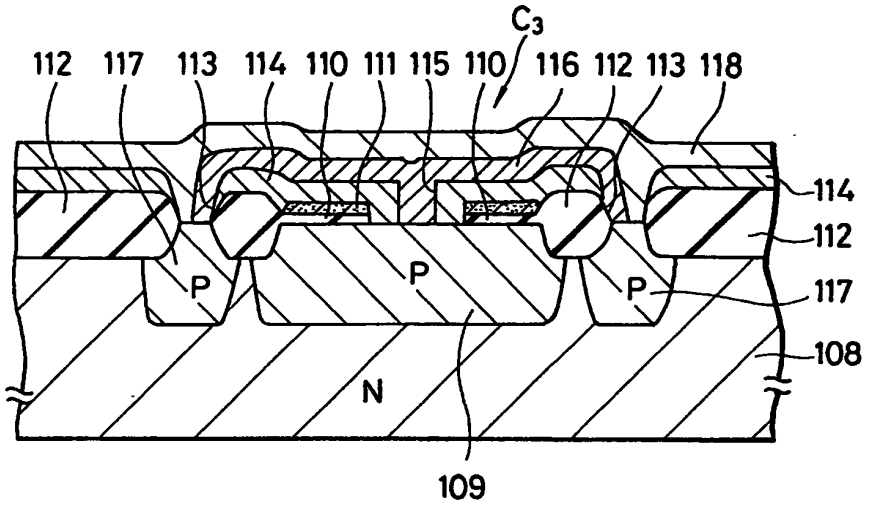

C3
112
117
113
114
110
111
115
110
116
112
113
118
114
112
117
108
P
P
P
N
109

FIG. 20

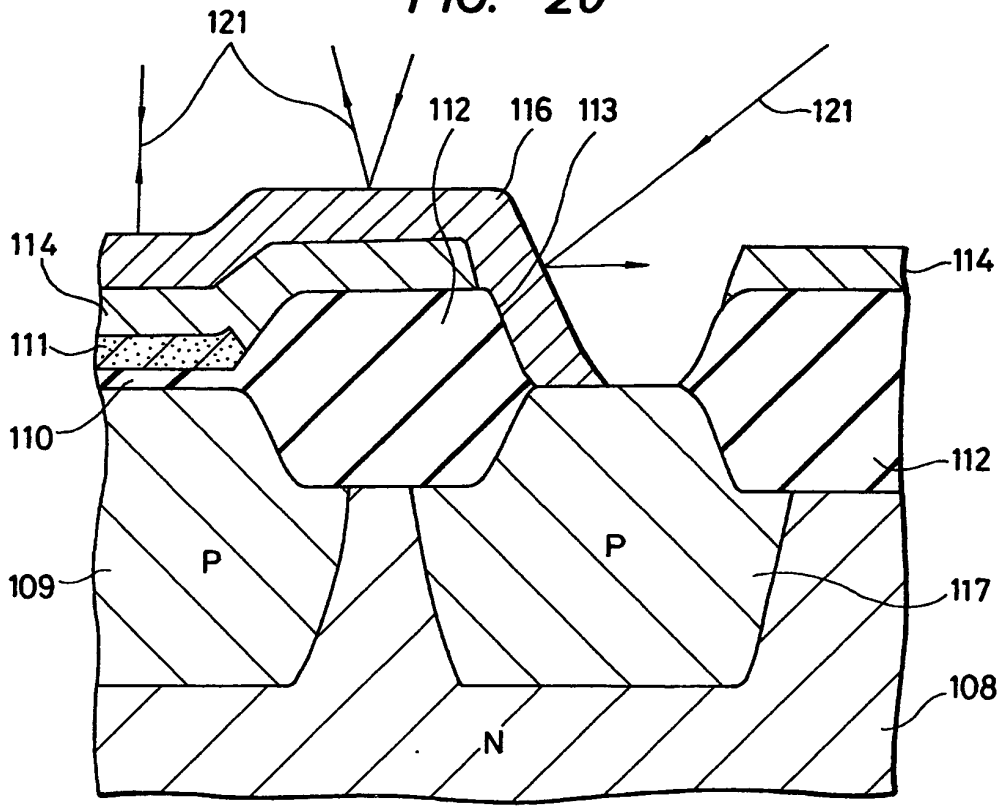

121
112
116
113
121
114
111
110
114
112
P
P
109
117
108
N

FIG. 21

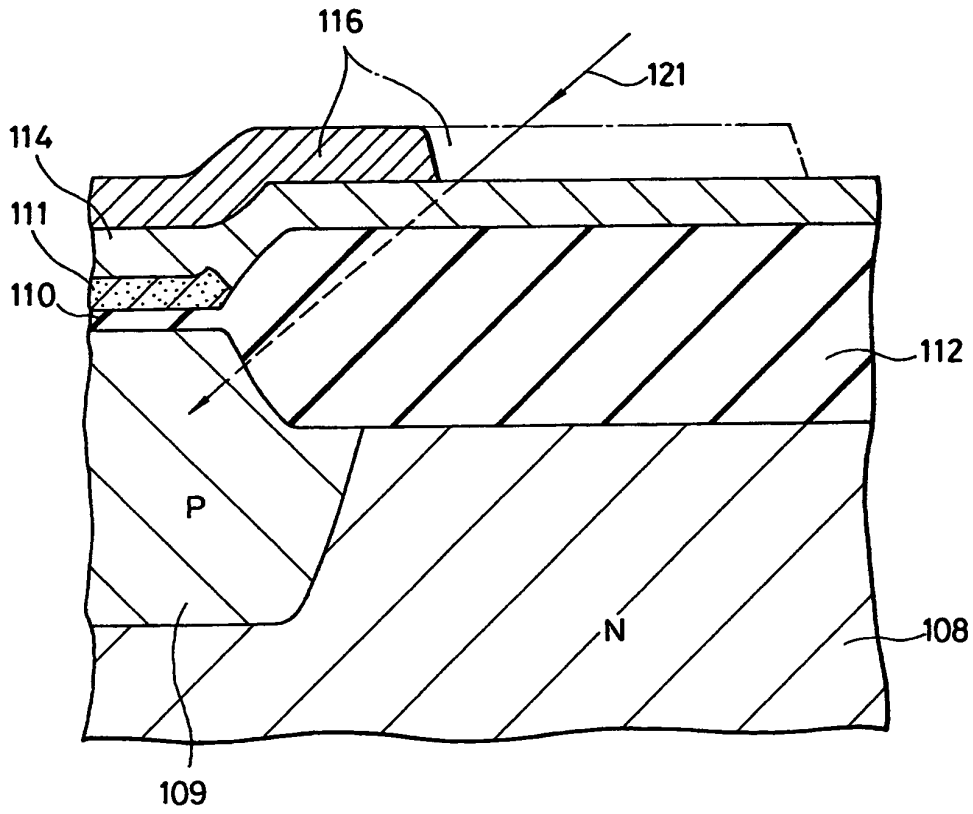


FIG. 22

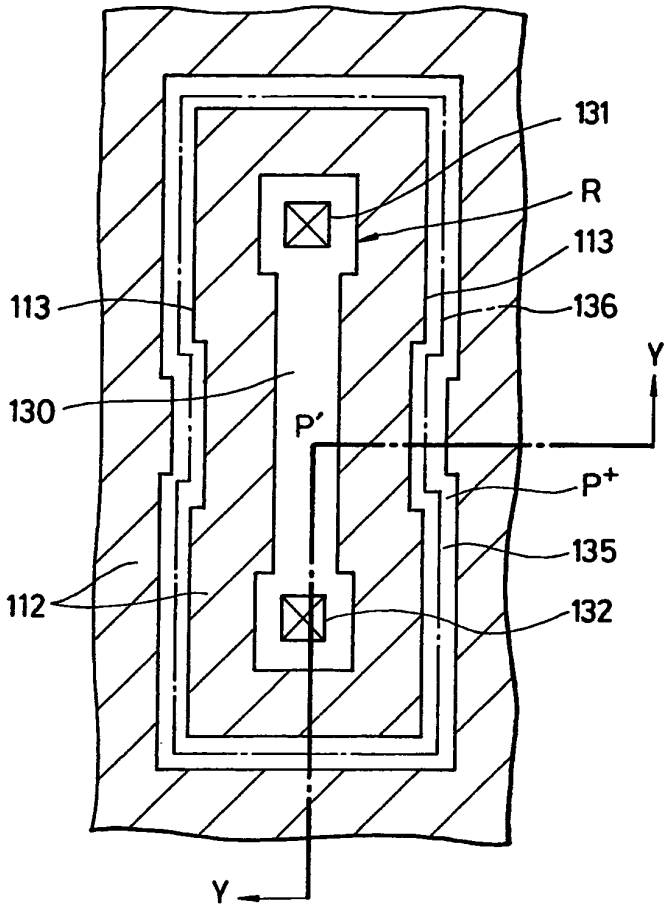

131
R
113
136
113
Y
130
P'
P+
135
112
132
Y

FIG. 23

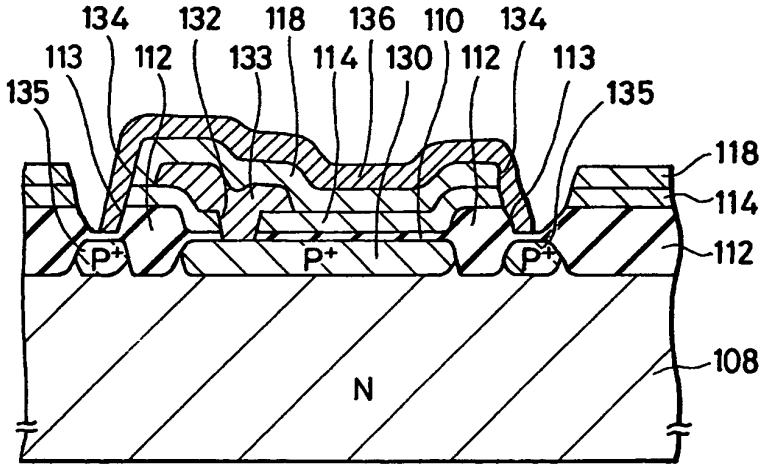

134
132
118
136
110
134
113
112
133
114
130
112
113
135
135
118
114
P+
P+
P+
112
108
N

FIG. 24

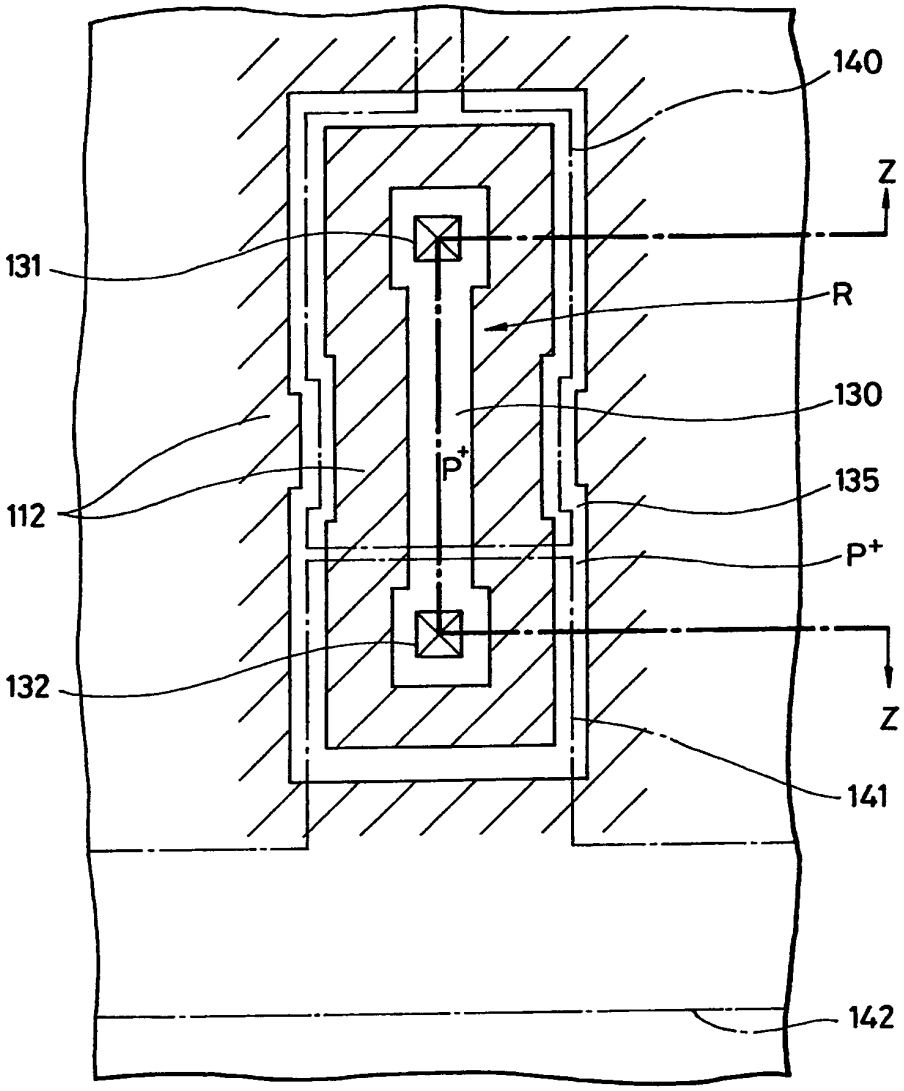


FIG. 25

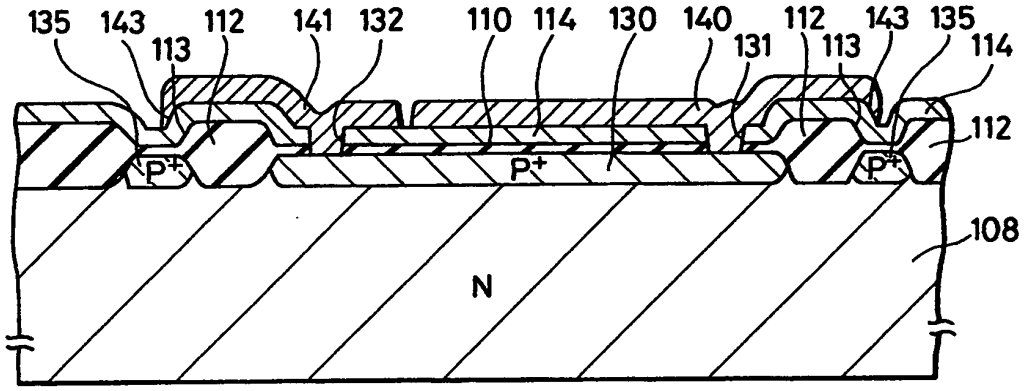
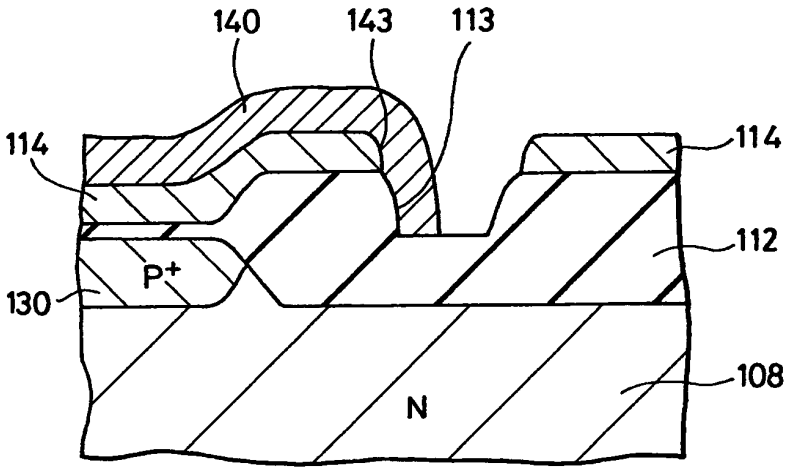

135
143
113
112
141
132
110
114
130
140
131
112
113
143
135
114
112
P+
P+
P+
108
N

FIG. 26


140
143
113
114
114
112
P+
130
108
N

SPECIFICATION

Semiconductor integrated circuit device

The present invention relates to a semiconductor integrated circuit device including MIS (Metal-Insulator-Semiconductor) type semiconductor circuit elements, and more particularly to a semiconductor integrated circuit device which is equipped with means for preventing malfunction due to irradiation with light.

A semiconductor integrated circuit device (which may be shortly referred to as an "IC") is usually formed by preparing circuit elements in a semiconductor substrate such as a single crystalline wafer of silicon by the circuit integrating technique and by packaging the complete semiconductor substrate in a package such as a ceramic type package or a resin mold type package so as to prevent it from being mechanically damaged from the outside. However, the semiconductor integrated circuit device thus completed may not necessarily require the final packing depending upon the electronic device it is to form part of. In an electronic watch, for example, an outer case such as the metal case of the electronic watch also acts as the protective case the semiconductor integrated circuit device so that the semiconductor integrated circuit device itself may not require an individual package. Rather, if the outer case of the electronic device can also act as the package of the semiconductor integrated circuit device, the production cost for the IC or the electronic device can be remarkably advantageously reduced.

From this standpoint, for the prior art in which the outer case of the electronic device can also be used as the protective case for the semiconductor integrated circuit device itself, it has been believed that there arises no problem if the package of the semiconductor integrated circuit device is simply omitted. Nevertheless, we, the Inventors, have found a problem that some semiconductor integrated circuit devices may be influenced by light, by the time the electronic device is completed, either when the circuit operation is inspected when the circuit operations of the electronic device incorporating the semiconductor integrated circuit device is adjusted. It has been found that the influences upon the circuit operation of the IC by light are especially dominant in ICs which include MIS or MOS (Metal-Oxide-Semiconductor) type circuit elements (both of which will be commonly referred to as "MIS type circuit elements") having high input impedance. Since, in MIS type ICs having no final package, the input impedances of the MIS type circuit elements, i.e., the insulated gate type field effect transistors are high, a leakage current is established at the PN junction forming the MIS type IC, when the MIS type circuit elements are irradiated with a light, while the impedances of the other circuit elements connected with the MIS type circuit elements are high, so that the leakage current due to the light obstructs the circuit operations of the IC.

MIS type ICs having an oscillator circuit ar especially liable to such circuit malfuncti ns caused by the light. Thus, the functions of the oscillator circuit are interrupted or the frequency f th oscillations is fluctuated by th light. That malfunction of the MIS typ IC caused by light is prevented by shielding the light, but the result is that the inspection of the circuit operations of the MISIC and the circuit adjustment of the electronic device making use of that inspection are remarkably complicated.

In order to make easily understandable the problems of the oscillator circuit of the MISIC, the influences of the light upon a MISIC having a watch circuit formed in a silicon substrate, especially a CMOSIC, will now be described with reference to the accompanying drawings.

Figure 1 shows the connection diagram of the respective circuit units of a watch circuit which is disposed in an IC chip 1 for an electronic watch. This IC chip 1 (i.e., the semiconductor chip) is equipped with an oscillator circuit 3 which has a quartz oscillator 2 between its input terminals A and B and which has its output terminal connected to a frequency divider circuit 4 and a driver circuit 5 driven by the frequency divider circuit 4 so that a signal for driving either a motor or a liquid crystal display device is fed out of the output terminal C of the driver circuit 5. From a power supply terminal D, on the other hand, there is supplied a power supply voltage which is fed to the driver circuit 5 and a voltage regulator 6. And, the power supply voltage to be fed to the oscillator circuit 3 and the frequency divider circuit 4 is stabilized by the voltage regulator 6.

Here, a circuit shown in Figure 2, for example, is used as the oscillator circuit 3. This circuit is disclosed in U.S.P. No. 4,100,502, for example, and is well known in the art. According to this oscillator circuit, reference letters Q_1 and Q_2 indicate a P-channel MISFET (i.e., P-channel insulated gate type field effect transistor) and an N-channel MISFET (i.e., N-channel insulated gate type field effect transistor), respectively, which constructs a CMOS inverter circuit. The gates of transistors Q_1,Q_2 are protected against excessive input voltages by an input protection resistor RD and a protection diode D. Letter C_1 indicates a trimmer capacitor for adjusting the oscillation frequency, and letter C_2 indicates a fixed capacitor. Both the MISFETs Q_1 and Q_2 are biased independently of each other by a coupling capacitor C_3 having a MIS type construction. On the other hand, P-channel and N-channel MISFETS Q_3 and Q_4 acting as bias resistors are connected between the respective gates and drains of the MISFETs Q_1 and Q_2. Between the FETS Q_1 and Q_2, on the other hand, there are connected current restricting resistors RL_1 and RL_2 which have their intermediate point connected with the terminal B. Numeral 7 indicates a wave forming circuit which is provided to convert the output waveforms of the CMOS inverter into a countable pulse form, and for this purpose P-channel and N-channel MISFETs Q_5 and Q_6 form together a complementary circuit.

If, in the oscillator circuit thus constructed, the input protection resistor RD, for example, is irradiated with light coming from the outside, a backward leakage current is established at the PN junction

between the P^+-type diffusion region and the N-type substrate forming that resistor by the electron-hole couples which are formed in the vicinity of the PN junction area. As a result, a leakage resistor $R\ell$ is equivalently incorporated, as shown in Figure 2. This leakage resistance is varied in accordance with the irradiation of the light. This leakage resistor has a relatively high resistance, but, since the input impedance of the MISFET Q_1 is higher than that, the bias voltage (i.e., the bias point) of the MISFET Q_1, which is determined by the ratio between the leakage resistance $R\ell$ and the bias resistance Q_3 is always varied in accordance with the surrounding condition. For example, if light is incident so that the leakage resistance $R\ell$ is reduced, the bias voltage V_G between the gate-source of the FET Q_1 is reduced so that the ocillation is made more difficult or is interrupted, as the case may be, or so that the oscillation frequency fluctuates. It is also found that the MIS capacitor C_3, which is formed in the P-type well area of the N-type substrate, is influenced by the light coming from the outside. As a result, leakage current due to the incident light is established at the PN junction between the P-type well and the substrate forming that capacitor and is fed as a leakage resistance R_ℓ', as shown in Figure 2. As a result, the bias voltage of the MISFET Q_2 is liable to fluctuate by the leakage resistance R_ℓ' so that phenomena similar to those mentioned above are caused. Incidentally, it is recognized that those influences by the external light also take place in the MISFETs Q_3 and Q_4 acting as the bias resistors. Even in the reference voltage generator circuit of the voltage regulator (refer to Figure 1), the fact that the oscillator circuit is influenced by the rise or drop of the output voltage due to the leakage current at that PN junction is recognized.

Thus, if the oscillator circuit is irradiated with light, the bias voltage of the amplification circuit forming the oscillator circuit is found to fluctuate.

Therefore, it is necessary that the oscillator circuit unit of the MISIC for the watch be shielded from external light. Incidentally, the IC chip is ordinarily packaged and therefore shielded when it is actually used as the final product in the watch case. However, if the IC chip is irradiated with external light when the circuit operations of the IC are checked before that packaging operation, especially, when the oscillation frequency is adjusted, the oscillation frequency fluctuates, as has been described hereinbefore, thereby causing a problem that the oscillation frequency becomes different when it is packaged for actual use in the outer case of the watch. In order to prevent this, it is necessary that the checking operations such as inspection or circuit adjustments before the packaging operation be performed under sufficiently shielded conditions. For example, it is conceivable that the chip and the measuring device themselves could be enclosed by suitable shielding means. This however is most inconvenient in practice, with the danger that the inspections and the adjustments cannot be precisely performed. Moreover, the shielding is liable to be insufficient so that the problem thus far described cannot be solved.

According to the present invention, the PN junction of at least a portion of circuit elements forming an oscillation circuit unit in an integrated circuit in a semiconductor substrate, is shielded from an external light by means of a shielding film.

More particularly, the invention provides a semiconductor integrated circuit device comprising:

circuit elements formed in one major surface of a semiconductor substrate, thereby to construct an oscillator circuit, said circuit elements including a PN junction which is formed in said one major surface, said circuit elements being so electrically connected with one another by interconnections which extend between them over said one major surface, as to provide at least part of the circuit arrangement of said oscillator circuit; and

a shielding film disposed over at least one of said circuit elements, which shields the PN junction of the circuit element from external light.

In the accompanying drawings:

Figure 1 is a schematic diagram showing an IC chip for an IC for an electronic watch, to which the present invention can be applied;

Figure 2 is an equivalent circuit diagram showing the oscillation circuit unit of the electronic watch IC chip shown in Figure 1;

Figure 3 is a schematic layout showing an IC chip which is formed with a shielding film according to the present invention;

Figure 4 is a partially enlarged top plan view example, in which a shielding film according to the present invention is formed in the oscillation circuit unit;

Figure 5 is a sectional view showing the major portion of oscillation circuit unit according to the present invention.

Figure 6 is a top plan view showing the coupling capacitor unit according to another example of the present invention;

Figure 7 is a section taken along line X - X of Figure 6;

Figure 8 is a top plan view showing an input protection resistor unit according to still another example of the present invention;

Figure 9 is a section taken along Y - Y of Figure 8;

Figure 10 is a top plan view showing an input protection resistor and a pad unit according to a modification of Figure 8 of the present invention;

Figures 11 and *12* show another modification of the present invention in a section taken along line X - X of Figure 12 and in a top plan view, respectively;

figures 13 and *14* show a further modification of the present invention in a section taken along line X - X of Figure 14 and in a top plan view, respectively;

Figures 15 and *16* show a further modification of the present invention in a section taken along line X - X of Figure 16 and in a top plan view, respectively;

Figure 17 is a schematic layout showing another embodiment of the IC chip for an electronic watch according to the present invention;

Figure 18 is a top plan view showing the coupling capacitor unit in the oscillator circuit of the IC chip shown in Figure 17;

Figure 19 is a section taken along line X - X of Figure 18 and includes a shielding film and a

passivati n film;

Figure 20 is a partial enlarged vi w of Figure 19 f r explaining the shielding condition;

Figure 21 is an enlarged sectional view similar to Figure 20 but shows a shielding structure which is used to explain the effects of the present embodiment;

Figure 22 is a top plan view showing an input protection resistor unit in the oscillator circuit of the IC chip shown in Figure 17;

Figure 23 is a section taken along Y - Y of Figure 22 but includes the interconnections and the shielding film;

Figure 24 is a top plan view showing an input protection resistor unit to be used in the IC chip of Figure 17 in accordance with a further embodiment of the present invention;

Figure 25 is a section taken along line Z - Z of Figure 24 but includes the interconnections which also act as the shielding film; and

Figure 26 is a partially enlarged sectional view showing the shielding structure according to the modification of Figure 25.

Description of the preferred embodiments

The present invention will now be described in detail with reference to the accompanying drawings of the embodiments thereof, in which it is applied to an MIS type IC for an electronic watch.

Figure 3 shows one embodiment of the present invention and is a schematic layout showing an IC chip which has the same circuit as the watch circuit of the IC chip shown in Figure 1. Reference numeral 1 indicates a silicon semiconductor substrate, and numeral 3 indicates an area, which is formed with an oscillator circuit which is constructed the same as that of Figure 2. Numerals 4, 5 and 6 indicate an area which is formed with a frequency divider circuit, an area which is formed with a driver circuit, and an area which is formed with a voltage regulator circuit, respectively, all of which are the same as the circuits shown in Figure 1 so they are indicated by the same numerals as those of Figure 1. On the other hand, the area 3 of the oscillator circuit shown in Figure 3 is constructed of the same circuit as that shown in Figure 2. Numeral 8 indicates external terminals, for example, bonding pads made of aluminium.

In the IC chip thus constructed, moreover, a shielding film 9, as indicated by hatched lines, is uniformly formed over the whole area of the respective circuit forming portions 3 to 6 in accordance with the present invention. This shielding film may be, for example, either a second aluminium film, which is formed on a first interconnection formed on the IC chip 1 to interconnect the circuit elements, or a third or subsequent aluminum film and may be another metal or insulating film having a shielding property. On the other hand, the shielding film 9 may be formed over only the oscillator circuit forming area 3, as shown in an enlarged scale in Figure 4.

Figure 5 shows the sectional construction f the oscillator circuit forming area 3 which is covered with the shielding film 9 shown in Figure 3 or 4. This Ic is an MISIC which has a LOCOS (Local Oxidation of Silicon) construction. More specifically, an N-type silicon substrate 10 is f rmed with the respective elements of Figure 2 and further with the second aluminum film 9 which has a thickness of about 2 μm and which is prepared all over the surface as a shielding film by the known vacuum evaporation technique. The input protection resistor RD is disposed at one element area, which is divided by a field oxide film 11 (LOCOS) grown to a thickness of about 1 μm on one major surface of the N-type substrate by local oxidation, and uses a P^+-type diffusion area 12 as the resistor RD. Numerals 13 and 14 indicate aluminum electrodes, which are disposed with a thickness of about 1 μm at both the ends of the resistor area 12, and an interconnection therefor, respectively. Numeral 15 indicates an oxide film which is formed simultaneously with the formation of a gate oxide film having a thickness of about 500 Å. Numerals 16 and 17 indicate phosphosilicate glass (PSG) films having a thickness of about 6,000 Å.

The coupling capacitor C_3 has one electrode formed by a P-type well 18, which is diffused relatively deeply into the substrate 10, the other electrode by a polycrystalline silicon film 19 which is formed over the first electrode to a thickness of about 4,000 Å, and a dielectric film of the oxide film 15 having a thickness of about 500 Å. The voltage supply to the polycrystalline silicon film 19 is performed by a first layer aluminum interconnection 20 having a thickness of about 1 μm.

Among the MISFETs Q_1 and Q_2 or Q_3 and Q_4, moreover, there are constructed both P-channel MISFETs, in which P^+-type diffusion areas 21 and 22 are used as a source and drain areas, respectively, and N-channel MISFETS, in which N^+-type diffusion areas 24 and 25 in a P-type well 23 are used as source and drain areas, respectively. Numerals 26 and 27 indicate polycrystalline silicon gate electrodes which are formed to have a thickness of about 4,000 Å on the gate oxide films 15 which have a thickness of about 500 Å. Numerals 28, 29, 30 and 31 indicate aluminum electrodes having a thickness of about 1 μm and interconnections therefor.

Thanks to the coverage of the whole surface of the oscillator circuit with the shielding film 9, such as ckecking the operation of the oscillator circuit or the whole circuit, adjustment of the oscillation frequency or the selection of the chip can be performed without darkening the surroundings before the IC chip is packaged or actually mounted in the outer case of the watch. In other words, even if an external light such as an illumination lamp exists in the surrounding, it is so effectively shielded by the shielding film 9 that it fails to reach the respective PN junctions therebelow. As a result, no leakage current is caused by incident light at the PN junction areas, and neither is there any effective leakage resistor round the input protection resistor and the coupling capacitor unit so that the characteristics of the bias resistors Q_3 and Q_4 and the FETS Q_1 and Q_2 do not fluctuate either. As a result, the oscillator circuit can be prevented from its malfunction and interruption of its functions due to th light. In the xample f Figur 3, moreover, sinc the regulator circuit f rming area 6 is also covered with the shielding film 9,

there is no leakag current ther either, making constant the output voltage of that regulator and the power which is consumed by th oscillator circuit 3, which is supplied with the v ltag from that regulator circuit, so that power is not unnecessarily consumed and so that the circuit operations can be stabilized.

Since the shielding film covers substantially all the surface of the ocillator circuit or chip which is liable to be influenced by the light, therefore, a sufficient shielding effect can be attained to prevent characteristic fluctuations due to leakage current, to facilitate or simplify the inspection of the IC chip or the circuit adjustment and the selection and to precisely perform the measurements. As a result, since the chip itself is shielded with the shielding film 9 even if the ocillation frequency, for example, is adjusted under the usual external light conditions, it is placed under an equivalent (or dark) surrounding condition as if it were packaged by the outer case so that it can be simply and precisely adjusted to the oscillation frequency for actual use.

According to another feature of the present example, moreoever, the chip itself including the oscillator circuit unit does not possess any function which prerequires the incidence of the external light but only such circuit units (especially the PN junctions of the constructing elements) at respective portions as are required to obviate that incidence, so that it is sufficient to cover the whole surface of the chip or the whole circuit unit raising the problem with the shielding film. Since especially the oscillator circuit unit is liable to experience fluctuations in the oscillation frequency by the influence of the light the fluctuations in the characterstics due to that incident light lead to degradation in the final electronic product, with the risk that the final product cannot function as an electronic watch. From this standpoint, the coverage of the oscillation circuit unit with the shielding film, as in the present example, has a remarkably important meaning. Moreover, since a watch IC chip molded with a resin is wholly packaged by the resin mold, the shielding effect by that mold is sufficient. However, that mounted product not of the mold type is held under the condition, in which the influences before the packaging by either the package of the IC chip or the outer case of the electronic device, i.e., the watch cannot be ignored. According to the present example, the shielding film thus far described is so constructed that it is formed on the surface of the chip itself thereby to exhibit prominent effects. This also means that tasks such as the adjustment before the packaging can be performed under the usual illuminating condition and that those tasks can be remarkably facilitated.

Moreover, when such an IC chip according to the present invention is used to produce an electronic device, a special package such as the resin type package need not be used for the IC chip but the outer case of the electronic device can also be used as the package of the IC chip so that the production cost of th el ctronic device can be reduced.

Another embodiment according to the present invention will n w be described with reference to Figures 6 and 7.

This mbodiment is constructed such that shielding means is disposed in the coupling capacitor forming portion described in the above and is different from that of Figure 5 in that the aluminium interconnection 20 is formed sufficiently widely for the shielding purpose and in that the second layer aluminium shielding film is omitted. More specifically, while the aluminium interconnection shown in Figure 5 has a normal width, as indicated by single-dotted lines 20 in Figure 6, in the present embodiment the interconnection itself is widened to an area sufficiently including the well, as indicated by solid lines 40. For example, the interconnection 40 is widened beyond the boundary of the P-type well area 18 by the width ℓ_1 of several tens of μm, thereby to sufficiently cover the bird beak portion 11a of the field oxide film 11. Incidentally, reference numeral 41 indicates a through hole, which is formed in the glass film 16 for connecting the interconnections 40 with the polycrystalline silicon film 19, and numeral 42 indicates a contact hole which is formed in the glass film 16 so as to supply the well 18 with the potential from an aluminium interconnection 43.

Thanks to the widening of the interconnection 40 itself for supplying the potential to the upper electrode 19 of the coupling capacitor C_3, the PN junction can be sufficiently widened while still being shielded from incident light. Therefore, an adequate shielding film can be formed merely by changing the mask pattern for etching the interconnection 40 without substantially changing the production process. According to this embodiment, it is unnecessary to dispose such an overlying aluminum shielding film as is shown in Figure 5. In particular, although the peripheral edge area of the diffusion area 18 and the polycrystalline silicon film 19 at the bird beak portion 11a are so constructed as to allow the light to incide without any difficulty, they are sufficiently shielded by the interconnection 40 thereby to raise no problem of leakage due to the incidence of light.

A further embodiment of the present invention will be described in the following with reference to Figures 8 and 9.

This example relates to the input protection resistor 12 of Figure 5. Power source lines 50 of aluminum in Figure 5 are so disposed along the resistor 12 as to partially overlap, as indicated by single-dotted lines in Figures 8 and 9, whereas the power souce lines in the present example are sufficiently windened in the transverse direction to the positions of the solid lines so that they are used as a shielding film 51. For example, the width of the shielding film 51 (i.e., the width $*_2$, as viewed from the diffusion area 12) may be several tens of μm to 50 μm, and the width of the power source lines 50 themselves are sufficient to be the overlap area with the diffusion area 12.

Since the power source lines 50 themselves are so extended in that way as to sufficiently cover the area including the resistor area 12 to be shielded, the present embodiment is advantag ous in that a shielding effect similar t that f th f reg ing embodiments can b attained and in that th shielding structur can be easily form d with ut any

change in the process of the prior art.

Figure 10 shows a modification of Figure 8.

According to this embodiment, in the contacting area between the bonding pad 8 of aluminum at the input side and the input protection resistor 12, aluminum films 60 at the side of the pad 8, as indicated by phantom lines, are further extended along the protection resistor 12 until they arrive, as an aluminum shielding film 61 thereover, at the vicinity of the other contacting area of the protection resistor 12. As a result, since the pad 8 itself can be made to sufficiently act as the shielding film merely by being extended, little spare area is wasted, and the production process thereof is simple.

Figures 11 and 12 show a further modification of the capacitor C_3 according to the present invention. The capacitor C_3 which has been described hereinbefore is shielded by an aluminum film 72 which extends over the polycrystalline silicon film 19 constructing one electrode of the capacitor and across the terminal portion 18' of the PN junction between the P-type well 18 and the N-type substrate. The aluminum film 72 acting as the shielding film contacts with the P-type well area 18 through a contact hole 71, which is formed in the phosphorous silicate glass film 16, and is used as the other electrode of the capacitor C_3. The polycrystalline silicon film 19 partially extends across a portion of the terminal portion 18' of the PN junction until it is electrically connected through a through hole 73 with an aluminum film 74 which is formed simultaneously with the aluminum film 72, The capacitor C_3 thus formed can be more completely shielded from the external light.

Figures 13 and 14 show a modification of the protection resistor RD according to the present invention. The P-type resistor area of the resistor RD has one of its terminals contacting through a contact hole 76 with a polycrystallline silicon film 78. The other terminal of the resistor area contacts with an aluminum film 77 through the contact hole 75 of the phosphorous silicate glass film 16. Moreover, that aluminum film 77 extends to cover the terminal portion of the PN junction between the substrate 10 and the P-type area 12 thereby to prevent the P-type area from being irradiated with any light. This construction can ensure more complete shielding effects than those having been described hereinbefore. According to this construction, the present invention can be easily applied to the conventional MISIC having a two-layered construction with the polycrystalline silicon layer and the aluminum layer.

Figures 15 and 16 show a further embodiment of the present invention and such a shielding structure for the MISFET as can be made by applying a process similar to the case of the embodiment shown in Figures 13 and 14. This MISFET is constructed such that the N-type semiconductor substrate 10 is formed therein with a P-type drain area 79 and a source area 80 and such that a gate insulating film 81 made of a silicon oxide film is formed between those areas, and a gate electrode 82 made of polycrystalline silicon is formed on that gate insulating film 81. With the source area 80, there is ohmically connected through a contact hol 87 a source electrode 83 which is mad of polycrystalline silicon. That source lectr d 83 is pr pared simultaneously with the polycrystalline silicon layer f th gate electrode 82. A phosphorous silicate glass film 84 is formed over the gate electrode 82 and the source electrode 83. Moreover, a drain electrode 85 of aluminum is formed to ohmically contact with the drain area 79 through the contact hole 86 of that phosphorous silicate glass film 84. Especially in the embodiment being described, the aluminum film disposed as that drain electrode 85 is formed to cover all the surfaces of the source and drain areas, as shown in Figure 16. That aluminum film 85 covers the PN junctions of the source and drain areas so that it acts as the shielding film. As a result, the source or drain area is prevented from being irradiated with any light. The MISFET thus prepared is adopted as the structure of the MISFET which constructs the oscillator circuit of the transistors Q_1 and Q_3, as shown in Figure 2.

A further embodiment of the present invention will now be described with reference to Figures 17 to 26.

According to the embodiment to be described hereinafter, at least those circuit elements of the semiconductor integrated circuit device as would be influenced by a light have depressed steps formed therearound, and a shielding film is formed to extend from the surfaces of those elements to the surfaces of the depressed steps so that the external light may be effectively reflected by that shielding film so as not to reach the elements.

Figure 17 is a schematic layout showing the MIS type circuit element forming areas to be used by the IC chip for the electronic watch. In Figure 17, reference numeral 101 indicates a silicon semiconductor substrate, which is formed with the same electronic watch circuit as that shown in Figure 1, and the same circuit portions as those of Figure 1 are indicated by the same reference numerals. Numeral 3 appearing in Figure 17 indicates an area which forms a MIS type circuit element and which has the same circuit construction as that of Figure 2. Numerals 4, 5 and 6 indicate an area forming the MIS type circuit element of the frequency divider circuit, an area forming the MIS type circuit element of the driver circuit, and an area forming the MIS type circuit element of the voltage regulator circuit, respectively. Of the circuit elements forming the oscillator circuit 3, especially those elements which are influenced by light, namely, the capacitor C_3, the resistor RD and FETS Q_3 and Q_4 are formed with shielding films 301, 302, 303 and so on according to the present invention. The shielding film need not necessarily be provided for all the circuit elements which might be influenced by light but may be disposed over at least the circuit elements which are highly influenced by the light so that substantially the necessary effect can be attained. According to the present invention, moreover, a shielding film 601 is also disposed for such a portion of the circuit element of th voltage regulator circuit 6 f r supplying the scillat r circuit 3 with th voltag as is liable to be influenced by the light. Incidentally, reference numeral 100 indicates bonding pads t be used as external terminals. The construction of the

shielding film disposed over the circuit lem nts which are liable to be influ nced by the light will b described in the following.

Figures 18 and 19 show an example, in which the shielding film according to the present invention is disposed in the coupling capacitor C_3 of the oscillator circuit 3. This coupling capacitor C_3 is of such an MIS construction as includes: a P-type well 109 which is formed on one major surface of an N-type silicon substrate 108 by the known diffusion technique; a thin gate oxide film 110 which is formed to grow on the surface of the P-type well 109 so that it acts as a dielectric film; and a polycrystalline silicon film 111 which is disposed as the other electrode on that dielectric film. It should, however, be noted that a surrounding, relatively thick field SiO_2 film 112 having a thickness of about 1 μm has a depressed step 113 all around the well 109, formed by a groove around the periphery of the well. The depth of the step 113 (i.e., the removed portion of the field SiO_2) is suitably about 0.5 μm. Moreover, an aluminum interconnection 116, which is formed on a phosphorous silicate glass film 114 over the well 109 in a manner to cover a through hole 115 thereby to act as the electrode of the P-type well 109, is extended over substantially all the surfaces of those elements in a manner to sufficiently cover the PN junction area between the well 109 and the substrate 108 and is extended into the depressed step 113. As a result, the aluminum interconnection 116 is extended not only to cover all the area of the capacitor C_3 but also to descend within the surround step 113 until it reaches the silicon surface. Incidentally, the portion of the substrate under the step 113 is formed with a P-type diffusion area 117 by the same diffusion step as the well 109, since the field SiO_2 film 112 is used as a mask, but that diffusion area 117 is not used at all. all. Numeral 118 indicates a second phosphorous silicate glass film layer. Numeral 119 indicates an aluminum interconnection which is disposed to apply a potential to the polycrystalline silicon film 111 and which is electrically connected with the polycrystalline silicon film 11 through a through hole 120 formed in the phosphorous silicate glass film 114 at the first layer.

As has been described hereinbefore, although the aluminum interconnection 116 is disposed to cover substantially all the surface of the coupling capacitor C_3 and to extend to the surrounding step 113, the usual interconnection technique can be applied, as it is, without any change in the process thereby to form such a shielding aluminum interconnection as exhibits sufficient shielding effects. More specifically, since the element as a whole is covered with the aluminum interconnection 116, external light 121 is completely reflected by this interconnection 116 even if it is incident upon the area overlying the aluminum interconnection 116, as shown in an enlarged scale in Figure 20, so that it does not enter into the element. As shown in Figure 20, moreover, since the aluminum interconnection 116 is ext nded ov r the step 113 surrounding the elem nt, the light is also reflected, by the aluminum 116 in the step 113 even it is going to bliquely enter the surrounding area, so that it also fails to reach the element. In other words, the sloped surface f the aluminum interconnection 116 occupying the step 113 acts t effectively reflect the external light 121 so that substantially no leakage current due to the incident light occurs at the PN junctions of the capacitor element. In the area outside of the step 113, on the other hand, the external lights partially enters into the silicon until it reaches the PN junction between the P-type area 117 and the substrate 118. Nevertheless, even if a leakage current is established at that PN junction, there arises no problem because the P-type area 117 itself is not used as any element.

On the other hand, the present example is so constructed that the field SiO_2 film 112 is partially removed along the periphery of the capacitor element so that it is shielded by the aluminum interconnection 116 which is extended into the recessed step 113. As a result, the position of the step 113 can be brought close to the well 109 while maintaining the shielding effect at a sufficient level. In other words, the width of the field SiO_2 film existing between the P-type areas 109 and 117 and the amount by which the aluminum film 116 extends beyond the capacitor element can be minimized to contribute to the high integration of the IC. More specifically, if the field SiO_2 film 112 surrounding the capacitor element were uniformly formed as is shown in Figure 21, the external light 121 would penetrate the capacitor element without any difficulty unless the interconnection 116 were elongate, as indicated by a single-dotted line, to extend beyond the field SiO_2 film 112 to give an adequate shielding action. In this case, therefore, the increase in the area occupied by the aluminum interconnection 116 would make the integration of the circuit disadvantageous. On the contrary, since the construction of the present example makes ingenious use of the step 113, as shown in Figure 20, a sufficient shielding effect can be attained without extending the aluminum interconnection 116 so much whereby an improvement in the integration can be accordingly expected.

Thanks to the formation of the shielding structure using the shielding film thus far described in such an element portion (i.e., the coupling capacitor in the present example) as is liable to be influenced by the light, tasks such as checking the circuit operation of the IC chip, adjustment of the oscillation frequency or chip selection can be performed without darkening the surroundings before the IC chip is packaged or actually mounted in the outer case of the watch without providing any package on the IC chip.

The following description referring to Figures 22 and 23 is directed to an example in which the present invention is utilised for the input protection resistor RD (refer to Figure 2).

This embodiment relates to the input protection resistor RD forming part of the oscillator circuit, as has been described hereinbefore. More specifically, the field SiO_2 film 112 for isolating the elements is made to selectively grow on one major surface of the N-type silicon substrate 108, and a P-type input protection resist r area 130 is form d in on l ment area by the known diffusion technique. Th oxide film 110, which is formed simultaneously with th gate oxide film, and the phosphorous silicate glass

film 114 have their respective contact holes 131 and 132 covered with th usual aluminum int rconnecti n 133. The field SiO_2 film 112 is formed with a removed portion which surrounds that resistor area 130 thereby to form the recessed step 113 similar to that of the foregoing embodiment. Moreover, the respective phosphorous silicate glass films 114 and 118 in the first and second layers are formed with a removed portion 134 so as to merge into that step 113, thus forming a deeper groove as a whole. Incidentally, numeral 135 indicates a P^+-type area which is formed by the same diffusion step as that of the resistor area 130 and which may be left as it is such that it is not used as a circuit element at all.

It is important here that not only the whole surface of the protecting resistor but also the surface of the step 113 is covered with an aluminum film 136 on the second layer so that the film 136 is used as the shielding film. With this construction thus described, a sufficient shielding effect can be attained by the aluminum film 136 by the reasoning similar to that of Figure 20 so that any leakage current caused by the incident light can be sufficiently prevented from being established at the PN junction between the P^+-type area 130 and the substrate 108. As a result, as before no discrepancy of the bias voltage is established, nor any fluctuation in the oscillation frequency due to leakage resistance.

Figures 24 and 25 show another embodiment of the present invention, which is developed from the foregoing embodiment having a recessed step, and the portions shared with the second embodiment are indicated by common reference numerals so that their repeated explanations are omitted here.

More specifically, this embodiment is characterized in that aluminum interconnections 140 and 141 connected with the respective terminals of the resistor area 130 so as to apply a potential thereto are made to have their widths enlarged so that they are used as the shielding films, respectively, and in that the one interconnection 141 is formed by elongating a portion of a grounding aluminum interconnection 142 which extends in the vicinity thereof. Those shielding films 140 and 141 are extended to the glass film 114 on the step 113 surrounding the element, but that glass film 114 is also formed with a step 143 following the contour of the step 113. As a result, a shielding effect as adequate as the aforementioned one can be attained by extending the interconnections 140 and 141 in that step 143. In the embodiment under discussion, moreover, the aluminum film provided is not separate of the element, but the aluminum interconnections 140 and 141 themselves are extended to be used as the shielding film. As a result, the shielding film can be formed merely by applying the usual interconnection step, as it is, without changing the production process. Moreover, since the one shielding film 141 is formed as a portion of the grounding interconnection 142, the area occupied by the distributing lines can b reduced to contribute to th improvement in the integration.

Figure 26 sh ws a modificati n f the embodiment just described.

Acc rding to this modification the field SiO_2 film 112 existing ar und the resistor area 130 is partially rem ved midway f its depth by the etching t chniqu thereby to f rm the step 113. Moreover, a step 143 corresponding to the step 113 is also formed in the overlying glass film 114 by the etching. Thus, if the aluminum interconnection 140 is extended, as shown, from the surfaces of all the elements into the steps 143 and 113, the penetration of light in the transverse direction can be so remarkably reduced that a sufficient sheilding effect can be attained. Incidentally, since the penetration of the light is dependent upon the depth of the step 113, it is desired that the depth be equal to or larger than about one half of the thickness of the field SiO_2 film 112 (nemaly, that the lower end of the step 113 be at the same or a lower position than the major surface of the substrate 8.

As is apparent from the description thus far made, since only the PN junctions of such elements of the ocillator circuit as are liable to be especially influenced by the light or the channel portions of the MISFETs may be covered with the shielding film thus far described, the oscillator circuit as a whole need not necessarily be covered with a shielding film. On the other hand, the construction of the oscillator circuit thus far described may be so variously modified that the gates of the CMOSFETs are directly connected, as disclosed in U.S.P. No. 3,855,549, for example.

When an electronic watch such as a wrist watch is to be produced by the IC chip thus far described according to the present invention, the following steps can be taken:

1. The step of mounting the parts such as the IC chip, the quartz oscillator, the trimmer capacitor or the fixed capacitor in the circuit substrate of a watch module thereby to prepare the module in which the watch circuit is completed. In this step, the IC mounting portion of the circuit substrate need not be packaged with either a resin or another package.

2. The step of operating the module, which has been prepared by the first step, by means of a battery so that the oscillation frequency of the oscillator circuit is adjusted to a predetermined level by adjusting the trimmer capacitor or the like. This circuit adjustment can be performed under any convenient external lighting condition without taking any special consideration of the influence of the external light.

3. The step of mounting the module, which has been subjected to the circuit adjustment, in the outer case of the watch. Thus, it is possible to complete the watch which has its circuit operations completely adjusted.

The electronic watch thus produced is remarkably advantageous even during the maintenance for replacement of the battery or the like. More specifically, when a portion of the outer case of the watch, e.g., the rear lid thereof is removed to replace the battery and the frequency is to be adjusted, this adjustment can be performed without taking any consideration of the influences of the external light with the portion of the outer case being opened. Thus, the watch using the IC chip according t the present invention can have its circuit adjustment

performed with remarkable ease.

Incidentally, the pres nt inv nti n can be applied not nly t the watch IC chip thus far described but als to an ther MISIC which is equipped with an oscillator circuit.

As has been described hereinbefore, according to the present invention, since the PN junction of at least a portion of the elements of the ocillator circuit unit is shielded by the shielding layer, the leakage current (or the leakage resistance) is prevented from being established at the PN junction by the incidence of the light so that the desired characteristic value, e.g., the desired oscillation frequency can always be set without any fluctuation. Moreover, since a sufficient shielding effect can be attained even with the presence of the surrounding external light, there arises no problem, even if the various works such as the adjustments or selections are performed under the usual illumination condition, so that they are made easy and accurate.

CLAIMS

1. A semiconductor integrated circuit device comprising:

circuit elements formed in one major surface of a semiconductor substrate, thereby to construct an oscillator circuit, said circuit elements including a PN junction which is formed in said one major surface, said circuit elements being so electrically connected with one another by interconnections which extend between them over said one major surface, as to provide at least part of the circuit arrangement of said oscillator circuit; and

a shielding film disposed over at least one of said circuit elements, which shields the PN junction of the circuit element from external light.

2. A semiconductor integrated circuit device as set forth in Claim 1, wherein said shielding film is an aluminum film.

3. A semiconductor integrated circuit device as set forth in Claim 1 or Claim 2, wherein said shielding film is formed over a plurality of the circuit elements.

4. A semiconductor integrated circuit device as set forth in any one of the preceding claims, wherein said shielding film is formed of a portion of said interconnection which is electrically connected with said circuit element to be shielded.

5. A semiconductor integrated circuit device as set forth in any one of the preceding claims, wherein said circuit elements include a field effect transistor connected to provide amplification, and a field effect transistor connected between the gate and the drain of said amplifying field effect transistor for providing bias; and wherein said shielding film is formed over said biasing field effect transistor.

6. A semiconductor integrated circuit device as set forth in claim 5, wherein there are two said amplifying field effect transistors, one of P-channel insulated gate type and one of N-channel insulated gate type, each having a respective said biasing field effect transistor of P-channel or N-channel insulated gate type.

7. A semiconductor integrated circuit device as set forth in Claim 6 wherein a capacitor f rming a said circuit element is connected betwe n the gates of said amplifying P-chann l and N-channel insulated gat type field ffect transistors.

8. A semiconductor integrated circuit device as set forth in Claim 7, wherein a shielding film is formed over said capacitor.

9. A semiconductor integrated circuit device as set forth in Claim 8, wherein the shielding film over the capacitor is formed by one electrode of said capacitor.

10. A semiconductor integrated circuit device as set forth in any one of claims 6 to 9, wherein a resistor forming a said circuit element is connected to the gates of said amplifying P-channel and N-channel insulated gate type field effect transistors.

11. A semiconductor integrated circuit device as set forth in Claim 10, wherein a shielding film is formed over said resistor.

12. A semiconductor integrated circuit device as set forth in Claim 11 wherein the shielding film over the resistor is formed by one electrode of said resistor.

13. A semiconductor integrated circuit device as set forth in any one of the preceding claims wherein a said shielding film is formed over a capacitor forming one of the circuit elements of the ocillator circuit.

14. A semiconductor integrated circuit device as set forth in any one of the preceding claims wherein a said shielding film is formed over a resistor forming one of the circuit elements of the oscillator circuit.

15. A semiconductor integrated circuit device as set forth in any one of the preceding claims wherein there is a step formed in an oxide layer on the surface of the substrate in the vicinity of the periphery of the circuit element over which the shielding film is formed, and the shielding film over the circuit element extends down over the step.

16. A semiconductor integrated circuit device as set forth in claim 15 wherein the step is formed by a peripheral groove recessed in the oxide layer.

17. A semiconductor integrated circuit device as set forth in claim 15 or claim 16 wherein the step substantially surrounds the circuit element.

18. A semiconductor integrated circuit device according to the invention and substantially as described herein with reference to the accompanying drawings.

19. An electronic watch fitted with a semiconductor integrated circuit device as set forth in any one of the preceding claims.

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